Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A micro-system for burning-in a ~~burn-in~~ system program from a plug-able subsystem into a main memory, comprising:

a processor for sending out a first control signal and a second control signal;

a main memory connected electrically with said processor for transferring data between said processor and said main memory;

a device for adjusting to a first ~~level~~ logic-level connected electrically with said processor for receiving said first control signal and connected electrically with said main memory for changing a logic-level ~~the level~~ of a third control signal to said [[a]] first logic-level ~~level~~ to enable said main memory; and

a plug-able subsystem with a backup memory connected electrically with said processor for receiving said second control signal, wherein ~~the~~ data are transferred between said backup memory and said processor when said second control signal is at said first logic level ~~level~~, and said plug-able subsystem sends out a forth control signal to said main memory for changing said third control signal to a second logic-level ~~level~~ to disable said main memory[[,]] ~~the~~ data are not transferred between said backup memory and said processor when said second control signal is at said second logic-level ~~level~~, and said third control signal is at said first logic-level ~~level~~ to enable said main memory for transferring data between said processor and said main memory.

2. (Currently Amended) The micro-system according to claim 1, wherein said second logic-level ~~level~~ is higher than said first logic-level ~~level~~.

3. (Currently Amended) The micro-system according to claim 1, wherein said device for adjusting to a first logic-level ~~level~~ includes a first grounded resistor.

4. (Currently Amended) The micro-system according to claim 1, wherein transferring data between said processor and said main memory includes the steps of:

establishing a first bus for transferring ~~the~~ address codes and a second bus for transferring ~~the~~ data codes between said processor and said main memory; and

transferring ~~the~~ data codes mapped to ~~the~~ address codes to the processor via said second bus after said main memory receives ~~receiving~~ a first read signal.

5. (Currently Amended) The micro-system according to claim 4, wherein transferring data between said processor and said main memory further comprises the step of:

writing ~~the~~ data codes mapped to ~~the~~ address codes to said main memory via said second bus after said main memory receives ~~receiving~~ a first write signal.

6. (Currently Amended) The micro-system according to claim 1, wherein transferring data between said processor and said backup memory includes the steps of:

establishing a ~~said~~ first bus for transferring ~~the~~ address codes and a ~~said~~ second bus for transferring ~~the~~ data codes between said processor and said backup memory; and

transferring ~~the~~ data codes mapped to ~~the~~ address codes to the processor via said second bus after said backup memory receives ~~receiving~~ a second read signal.

7. (Currently Amended) The micro-system according to claim 6, wherein said plug-able subsystem comprises:

a connector connected electrically with said processor and said main memory; and

a device for adjusting to a second logic-level ~~level~~ connected electrically with said connector for sending out said forth control signal through said connector to change a logic-level ~~the level~~ of said third control signal to said second logic-level.

8. (Currently Amended) The micro-system according to claim 7, wherein said device for adjusting to a second logic-level ~~level~~ includes a second resistor connected to a power supply.

9. (Original) The micro-system according to claim 7, wherein said connector is a slot.

10. (Original) The micro-system according to claim 1, wherein said main memory is a non-volatile memory.

11. (Currently Amended) A method for burning-in a ~~burn-in the~~ system program from a plug-able subsystem into a main memory in a micro-system, wherein said micro-system includes a processor, ~~said~~ a main memory, a device for adjusting to a first logic-level ~~level~~ to enable said main memory, and said plug-able subsystem with a backup memory, comprising the steps of:

sending out a first control signal for changing a logic-level ~~the level~~ of a third control signal and a second control signal to said plug-able subsystem from said processor, wherein a logic-level ~~the level~~ of said second control signal level is at a first logic-level ~~level~~ to enable said plug-able subsystem, and a logic-level ~~the level~~ of said third control signal is changed to said first logic-level ~~level~~ by said device for adjusting to a first logic-level ~~level~~;

sending out a forth control signal from said plug-able subsystem for changing the logic-level ~~level~~ of said third control signal to a second logic-level ~~level~~ to disable the main memory;

transferring data between said backup memory and said processor;

sending out said second control signal to said plug-able subsystem from said processor, wherein said second control signal is at said second logic-level ~~level~~ to disable the plug-able subsystem and said forth control signal is not sent out from said plug-able subsystem again; and

transferring data between said main memory and said processor.

12. (Currently Amended) The method according to claim 11, wherein said second logic-level ~~level~~ is higher than said first logic-level ~~level~~.

13. (Currently Amended) The method according to claim 11, wherein said device for adjusting to a first logic-level ~~level~~ includes a first grounded resistor.

14. (Currently Amended) The method according to claim 11, wherein transferring data between said processor and said backup memory includes the steps of:

establishing a first bus for transferring ~~the~~ address codes and a second bus for transferring ~~the~~ data codes between said processor and said backup memory; and

transferring ~~the~~ data codes mapped to ~~the~~ address codes to the processor via said second bus after said backup memory receives ~~receiving~~ a second read signal.

15. (Currently Amended) The method according to claim 11, wherein transferring data between said processor and said main memory includes the steps of:

establishing a ~~said~~ first bus for transferring ~~the~~ address codes and a ~~said~~ second bus for transferring ~~the~~ data codes between said processor and said main memory; and

transferring ~~the~~ data codes mapped to ~~the~~ address codes to the processor via said second bus after said main memory receives ~~receiving~~ a first read signal.

16. (Currently Amended) The method according to claim 15, wherein transferring data between said processor and said main memory further comprises the step of:

writing ~~the~~ data codes mapped to ~~the~~ address codes to said main memory via said second bus after said main memory receives ~~receiving~~ a first write signal.

17. (Currently Amended) The method according to claim 14, wherein said plug-able subsystem further comprises:

a connector connected electrically with said processor and said main memory; and

a device for adjusting to a second logic-level ~~level~~ connected electrically with said connector for sending out said forth control signal through said connector to change a logic-level ~~the level~~ of said third control signal.

18. (Currently Amended) The method according to claim 17, wherein said device for adjusting to a second logic-level ~~level~~ has a second resistor connected to a power supply.

19. (Original) The method according to claim 17, wherein said connector is a slot.

20. (Original) The method according to claim 11, wherein said main memory is a non-volatile memory.